# 100 nm Gate Length High Performance Low Power CMOS Transistor Structure

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Portland Technology Development, *QRE, #TCAD

Intel Corporation

1999 IEDM

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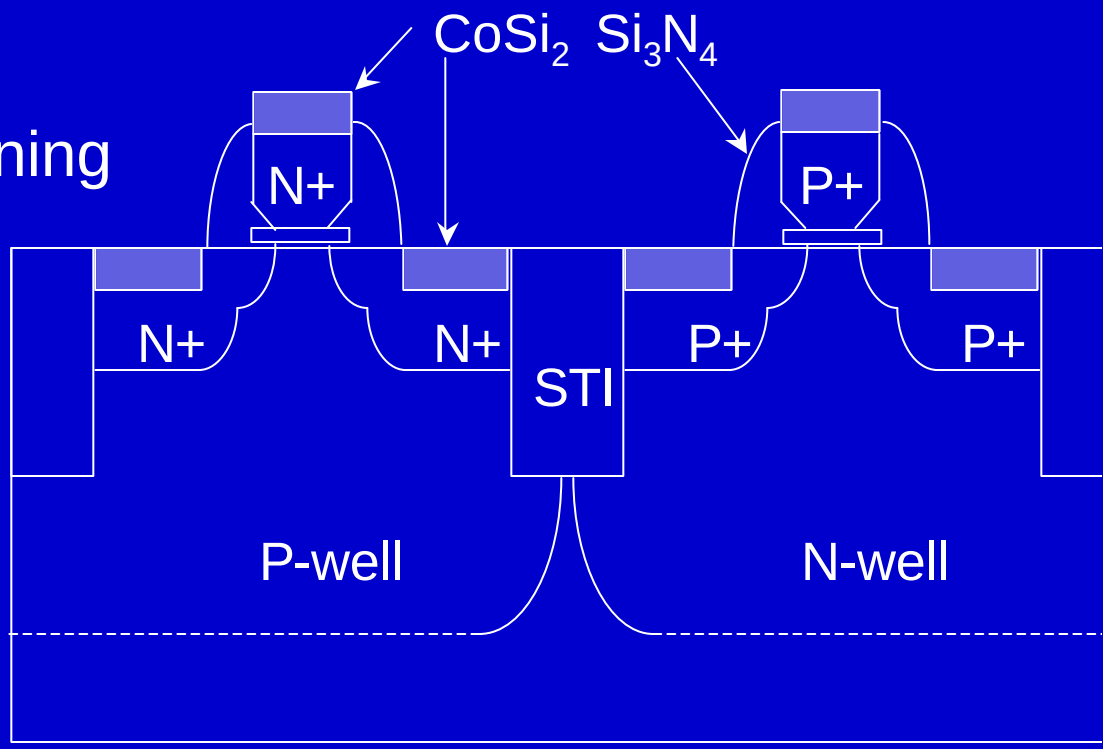
# Outline

- Transistor Features
- Transistor Parametrics
- Performance Benchmarking
- Conclusions

# Front End Process Flow and Features

- Shallow Trench Isolation
- Well & $V_{TH}$ Adjust Implants
- Gate Oxide Formation
- Notched Poly Gate Patterning
- Shallow Tip extensions
- Angled Halo Implants
- $Si_3N_4$ Spacer
- Deep Source/Drain
- Co Salicide
- 1.2~1.6 Volt Operation

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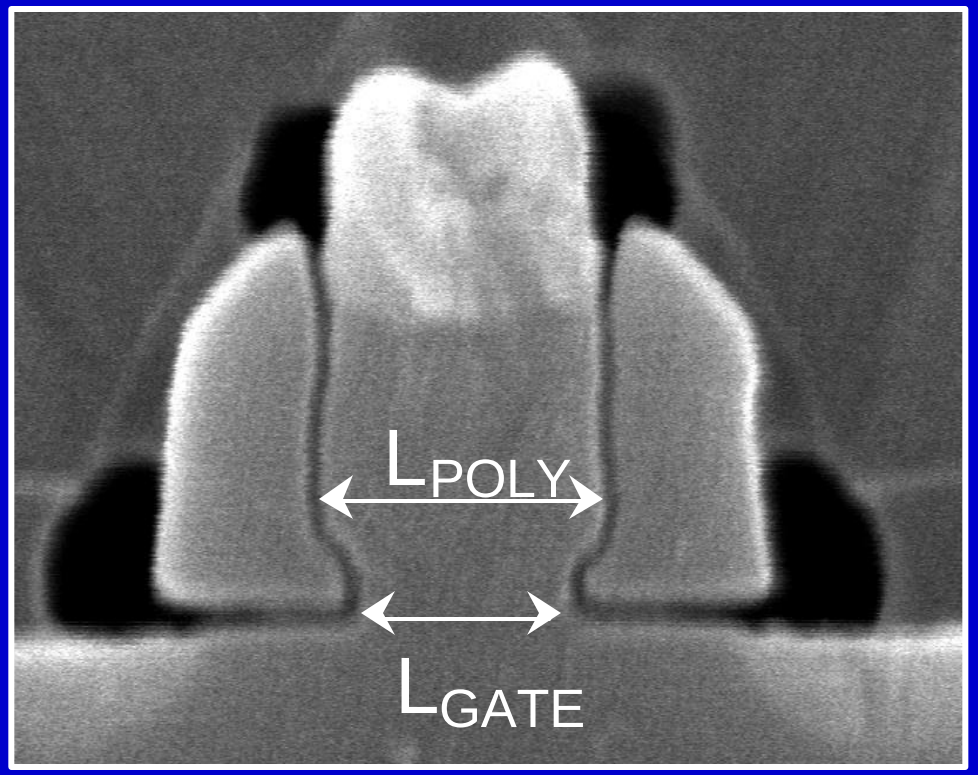
# Key Transistor Features Impacting Performance

- Notched Poly Profile
- Well Halo Optimization
- 2nm Physical Gate Oxide
- Junction Capacitance Minimization
- Cobalt Silicide

# Notched Poly Profile

- Advantages of Poly Notch:
  - $C_{GATE}$ reduction
  - Lower salicide resistance at a given $L_{GATE}$
  - High $I_{DSAT}$ at low Miller Cap
- Cost-Free Process
- $L_{POLY}$ =130nm
  $L_{GATE}$= 100nm

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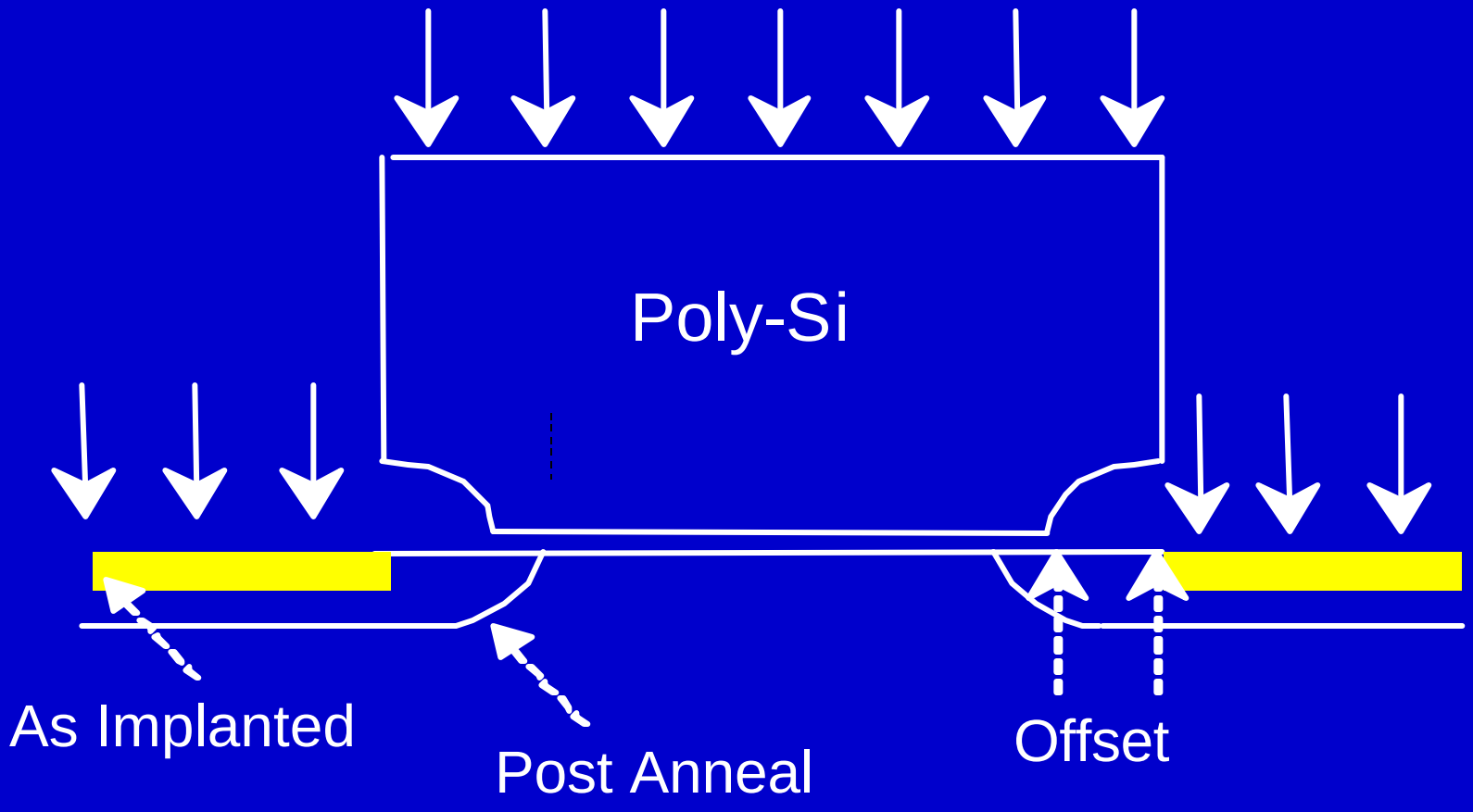
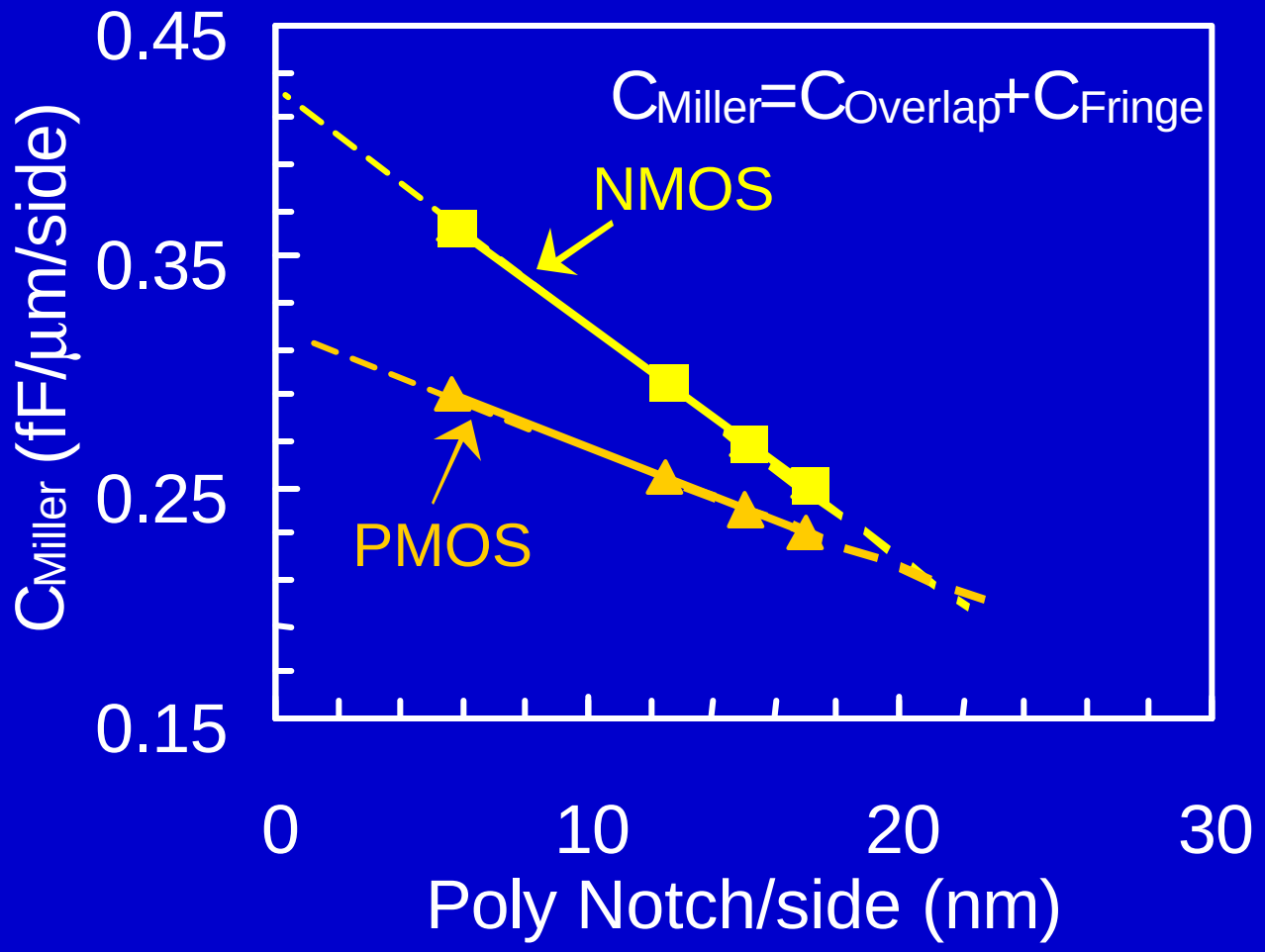
# SDE Formation with Poly Notch



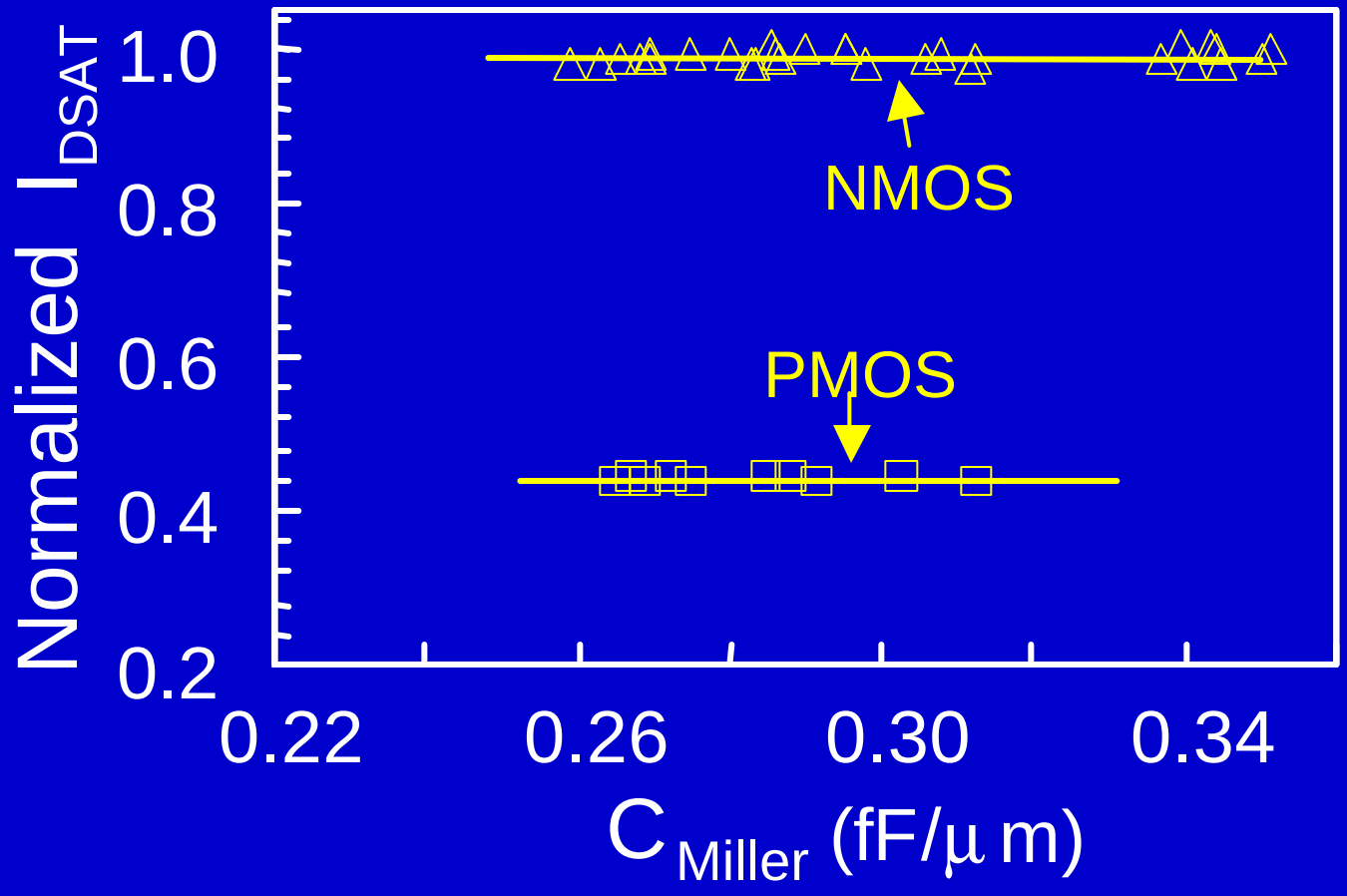

- Heavily doped SDE regions obtained at minimal under-diffusion

# $C_{MILLER}$ Modulation with Poly Notch




- $C_{MILLER}$ modulates linearly with poly notch size

# $I_{DSAT}$ vs. $C_{MILLER}$ Characteristics




- High $I_{DSAT}$ demonstrated at low $C_{MILLER}$ with "Notched-Poly" process

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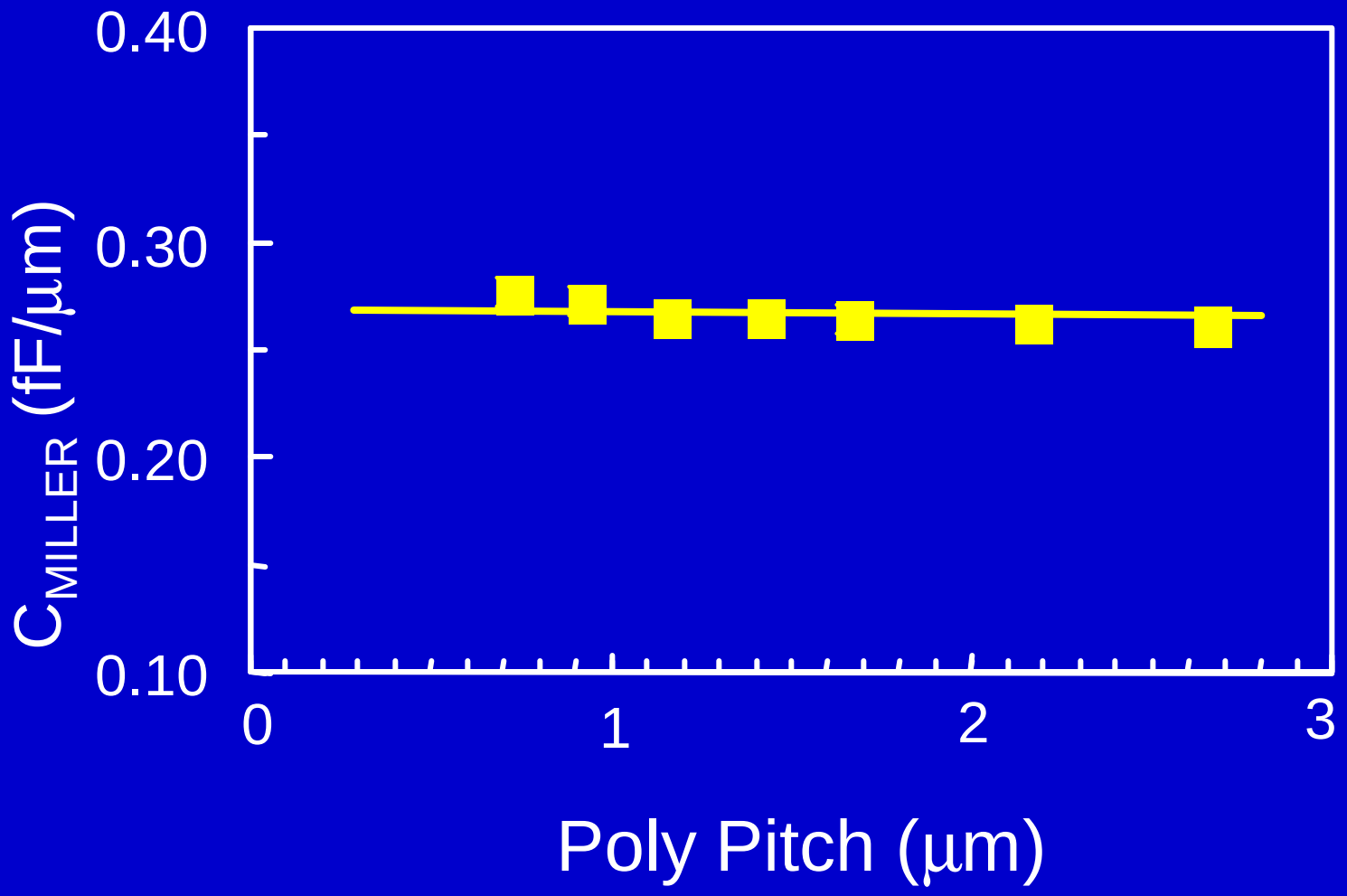
# Poly Notch Process Control




- Poly notch dimension is insensitive to poly pitch

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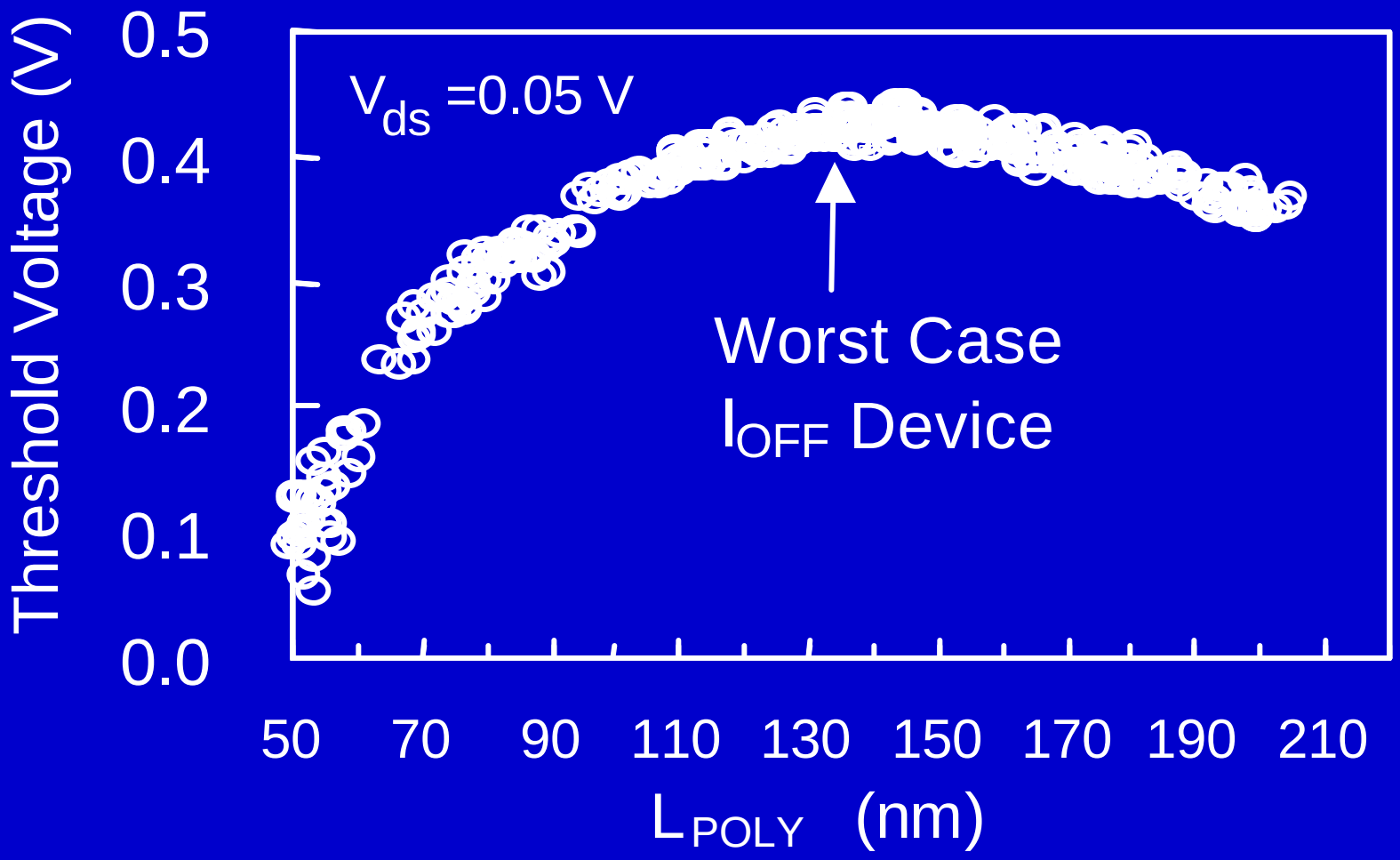
# Well-Halo Optimization




- Well Halo combination optimized to minimize performance degradation between worst case & target devices

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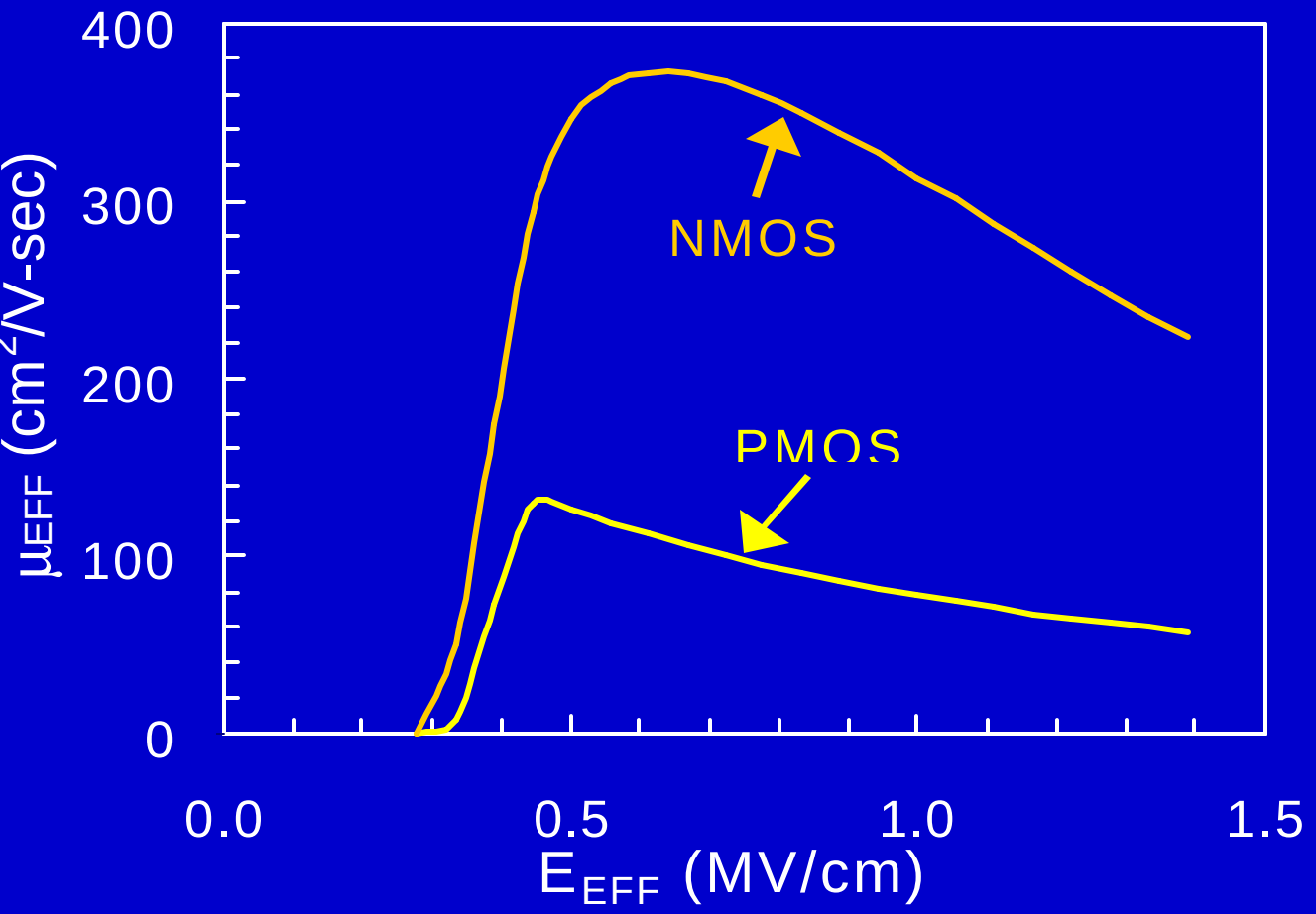
# Electron and Hole Channel Mobility




- High NMOS & PMOS mobility demonstrated for devices with 2nm thick physical oxide

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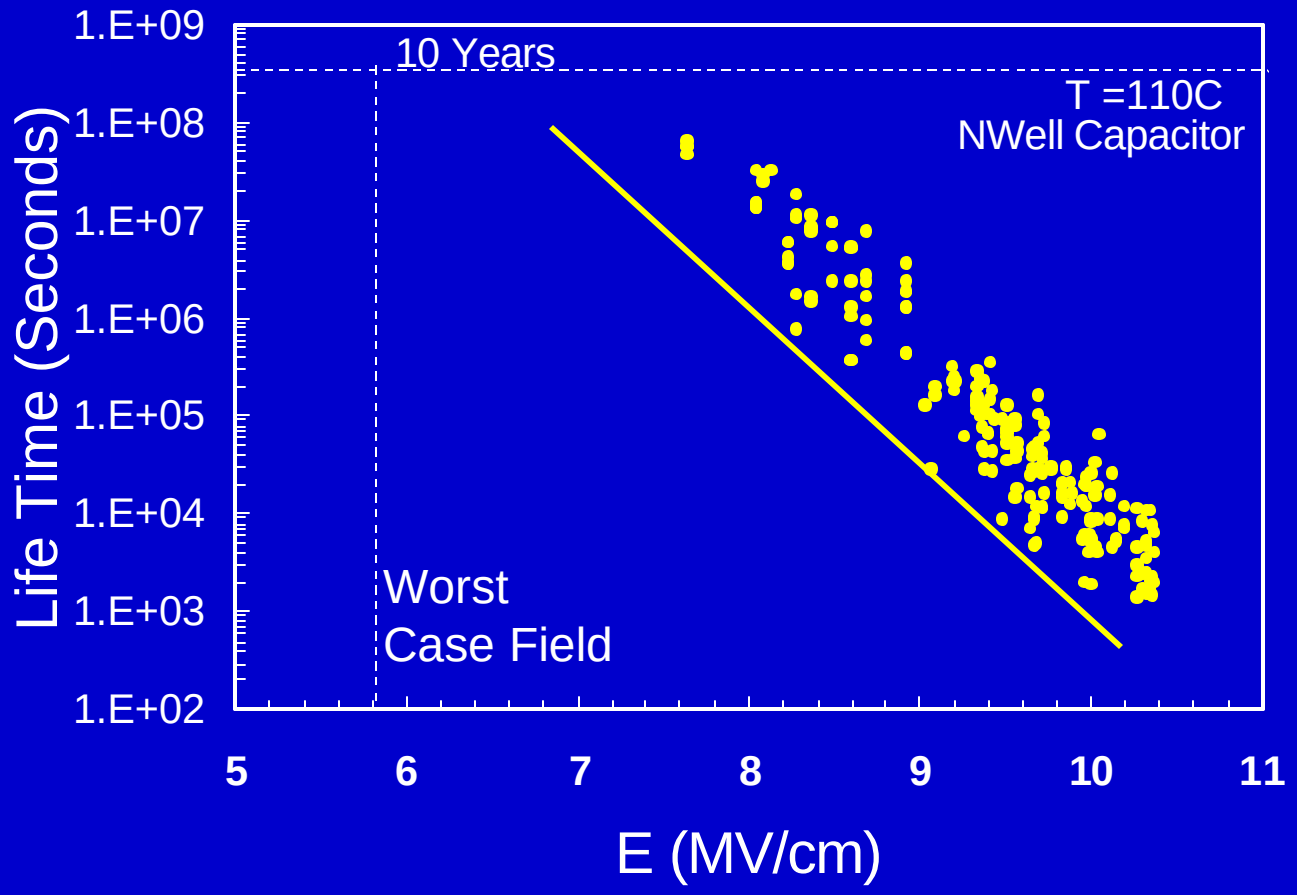
# 2nm Physical Gate Oxide Lifetime




- Some data points correspond to 1.5 years stress
- Product $V_{CC}$ is set based on oxide area and temperature
- Gate oxide meets 10 years life time criteria

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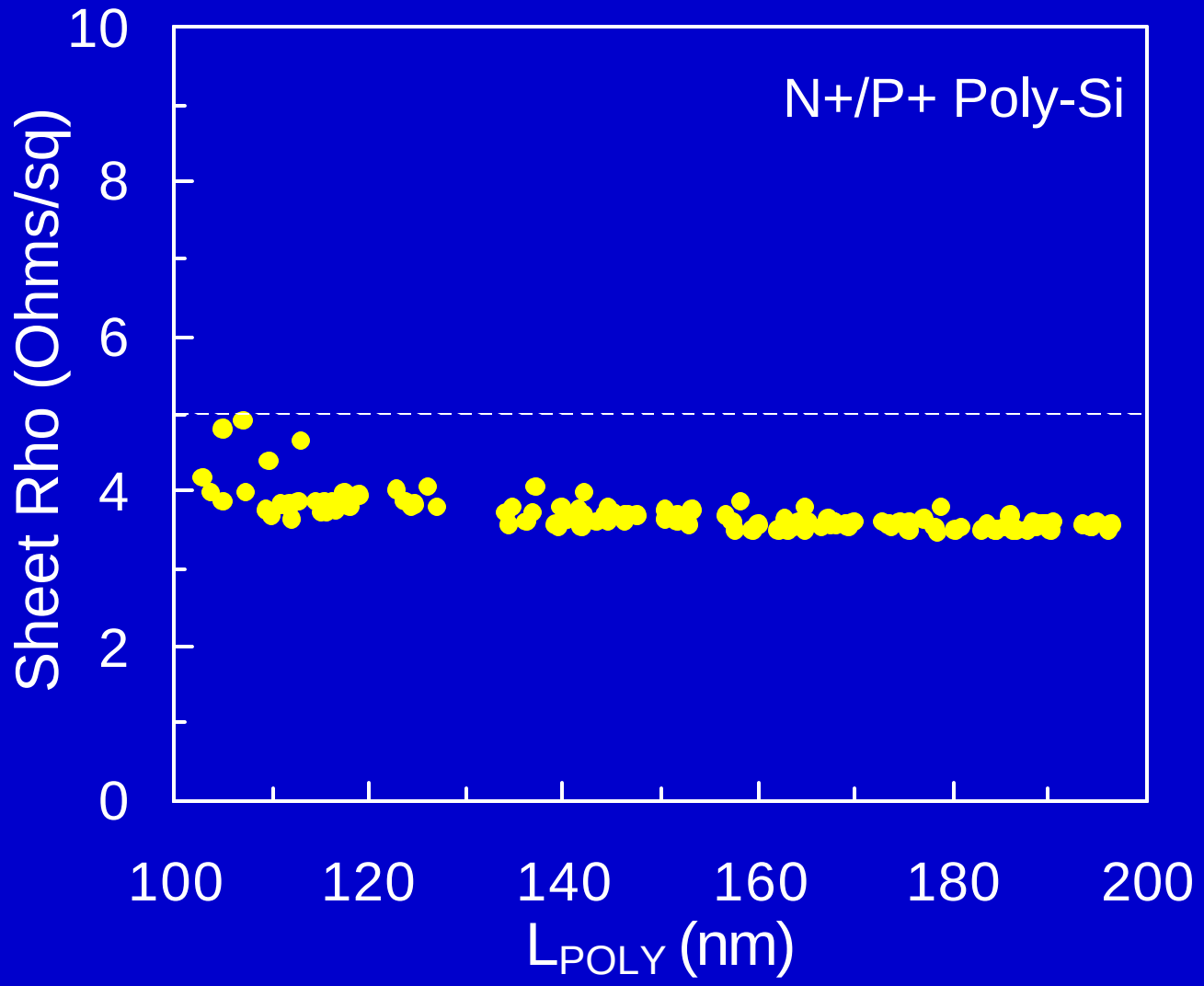
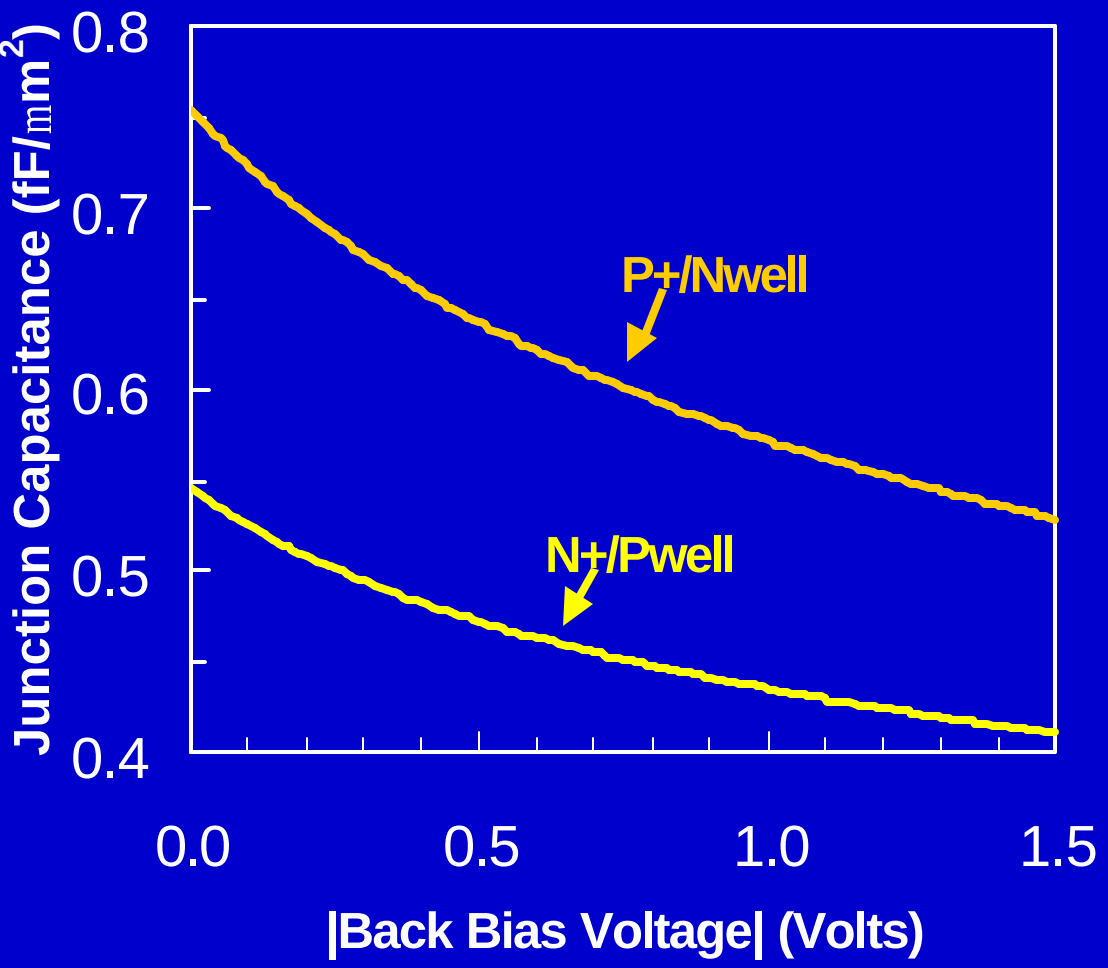
# Co Salicide Electrical Results



# Area Junction Capacitance




- Very low $C_{JA}$ achieved without compromising isolation

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- Transistor Features
- **Transistor Parametrics**
- Performance Benchmarking
- Conclusions

# Transistor Parameters Summary

| | 1998 IEDM | | This Work | | |
|---|---|---|---|---|---|
| | NMOS | PMOS | NMOS | PMOS | |
| $L_{POLY}$ | 130 | 150 | 130 | 135 | nm |
| $V_T$ (at 1.5V $V_D$) | 290 | -230 | 290 | -230 | mV |
| $I_{D\_SAT}$(at 3 nA $I_{OFF}$) | 0.94 | 0.42 | 1.04 | 0.46 | mA/um |
| $C_{MILLER}$ | 0.27 | 0.24 | 0.27 | 0.24 | fF/um |
| $C_J$ (at 0V bias) | 0.65 | 0.80 | 0.55 | 0.75 | fF/um$^2$ |

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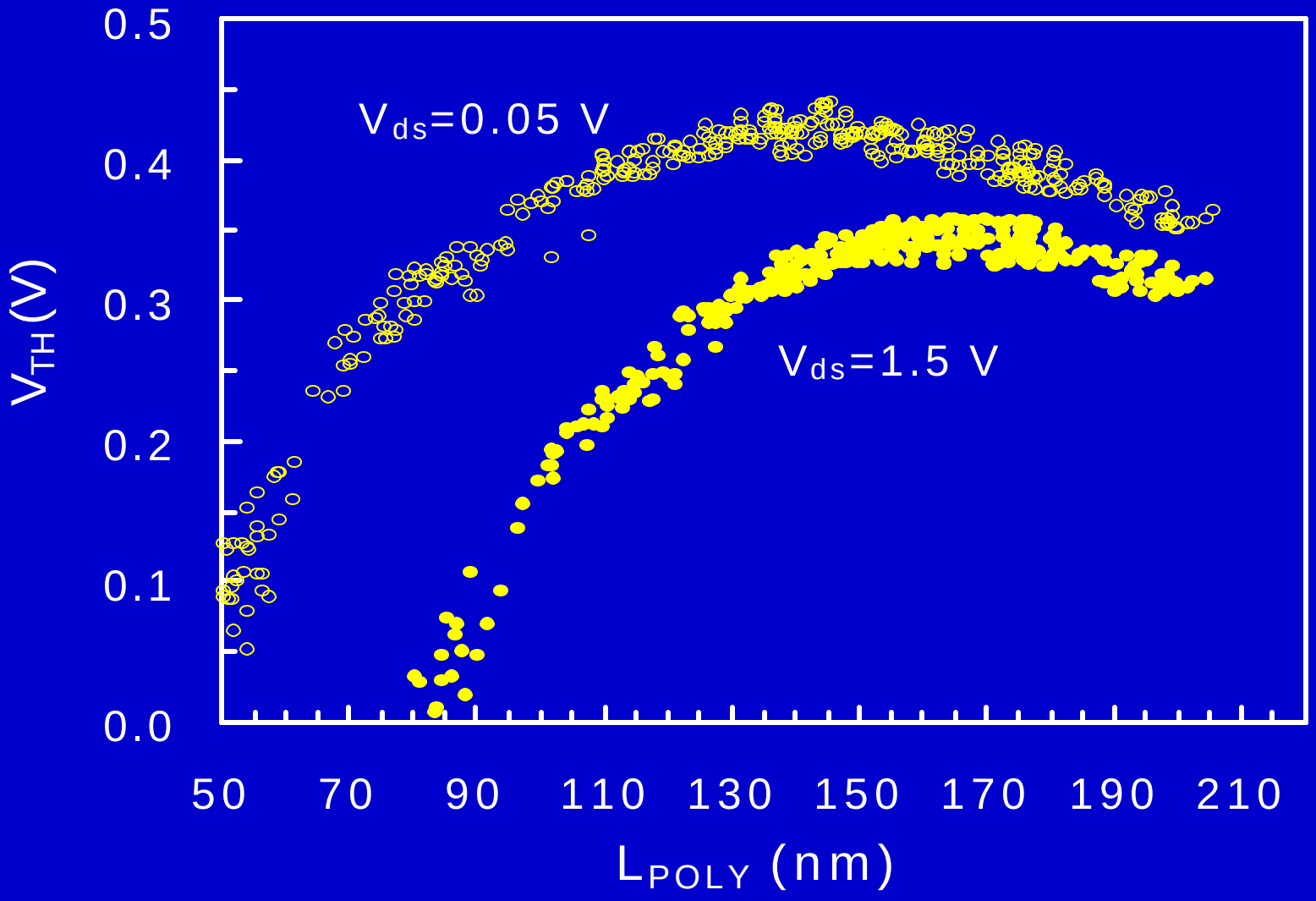
# NMOS $V_T$ vs. $L_{POLY}$

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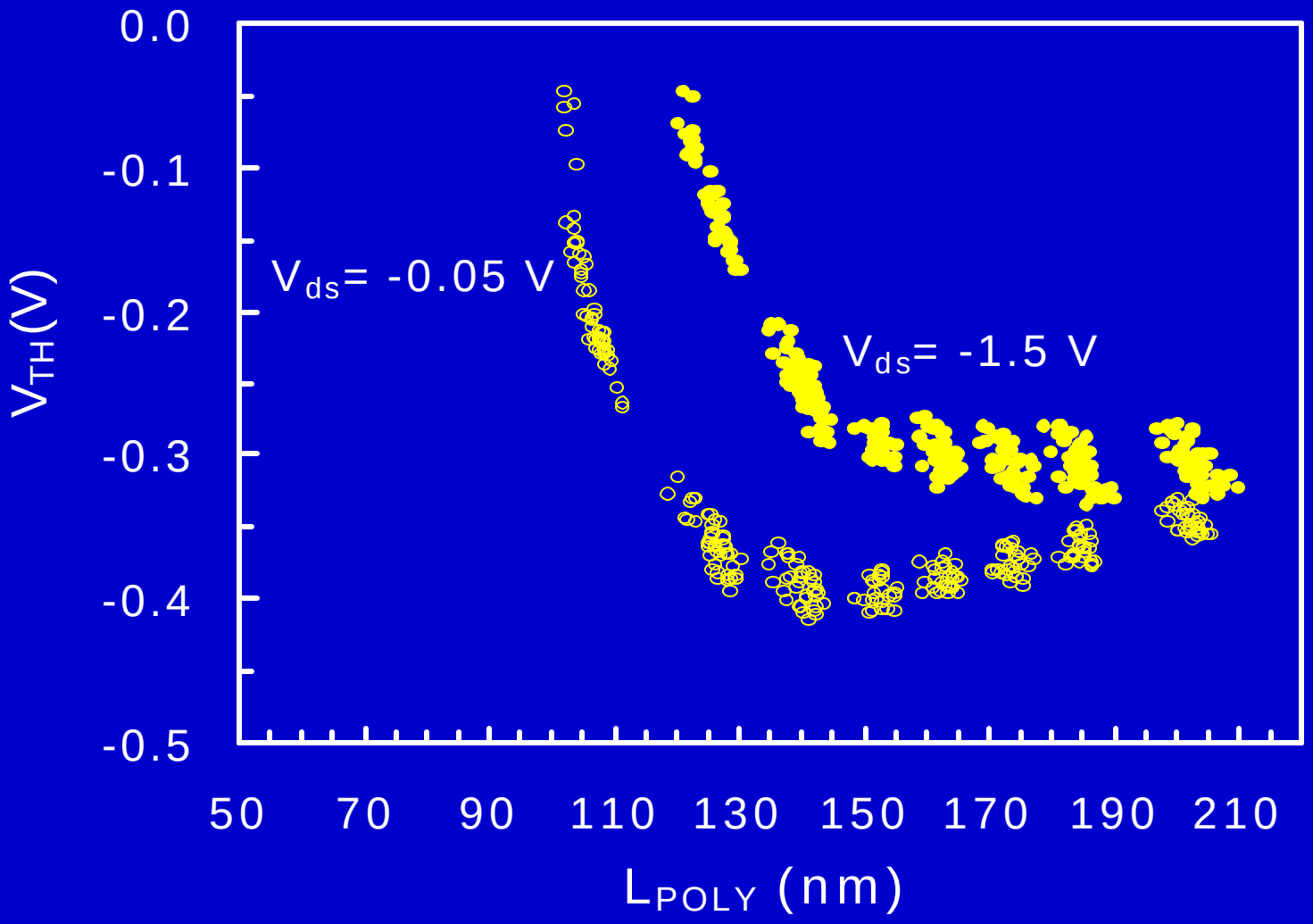
# PMOS $V_T$ vs. $L_{POLY}$

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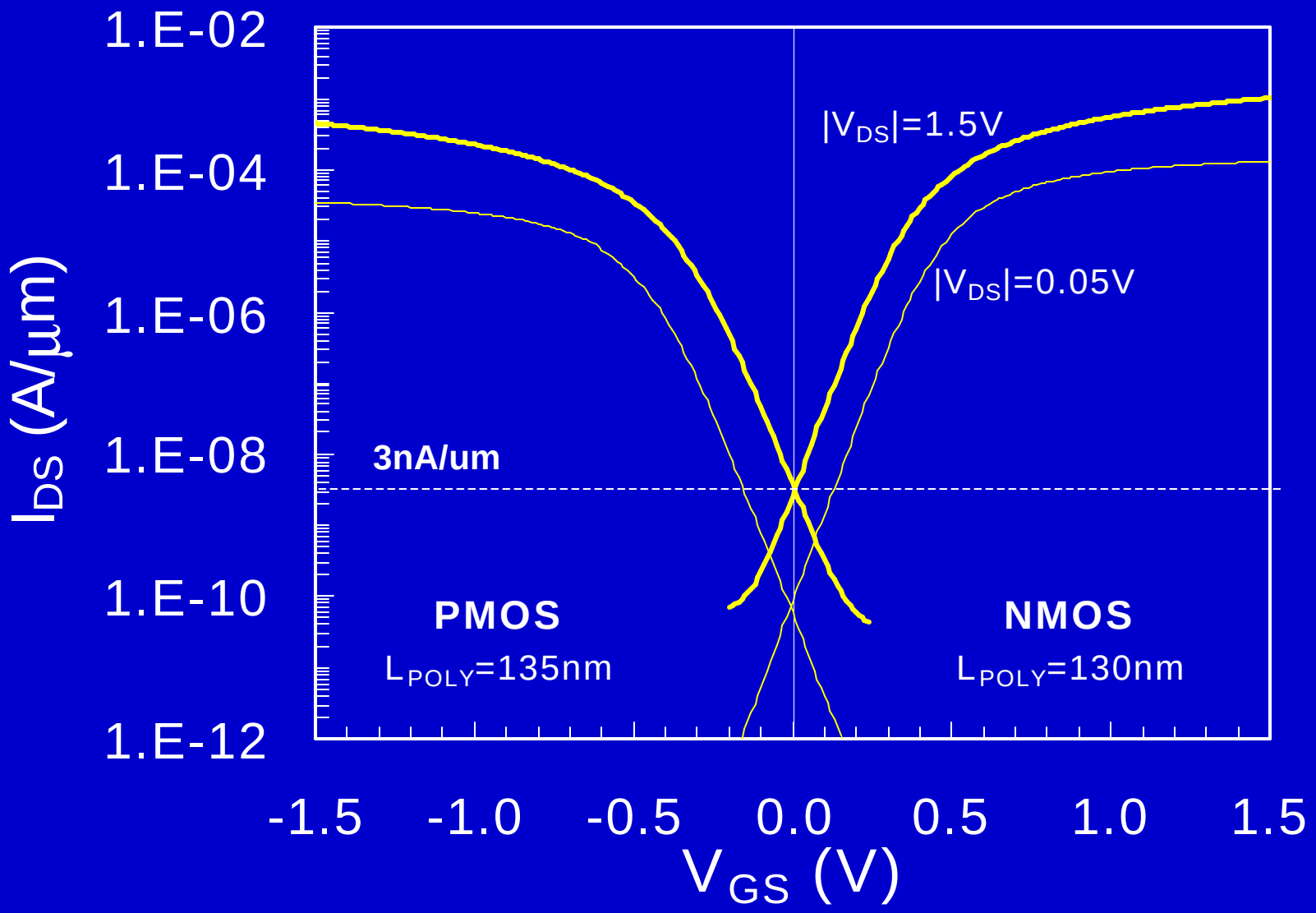
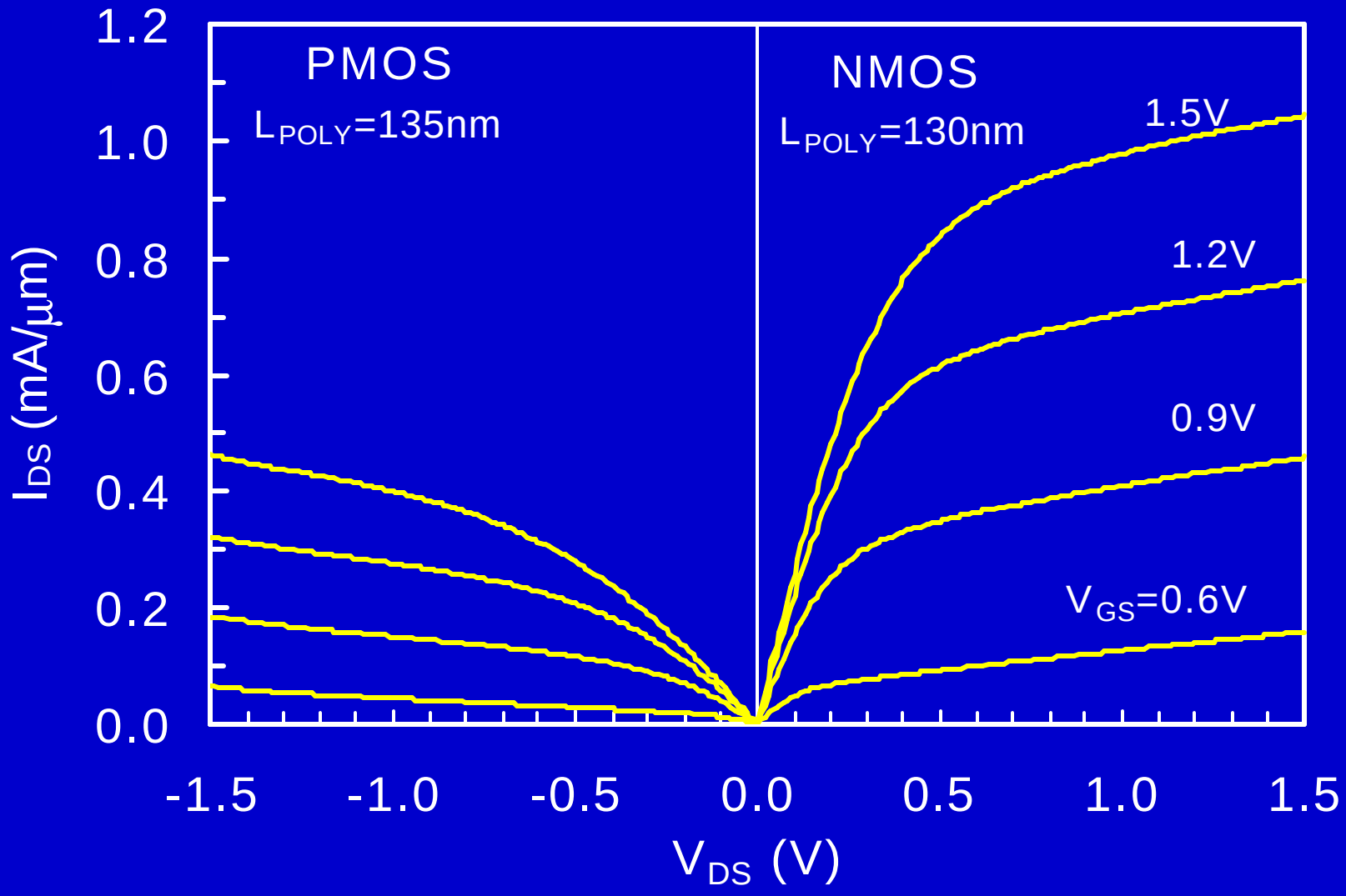
# Sub-threshold Characteristics



# Transistor I-V Characteristics



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- SRAM Performance
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# Performance Metrics

- Drive Current vs Off Current ($I_{ON}$ vs $I_{OFF}$)
- $C_g V_d / I_d$ Gate Delay
- Energy-Delay Product
- FO=1 Ring Oscillator Delay
- SRAM performance

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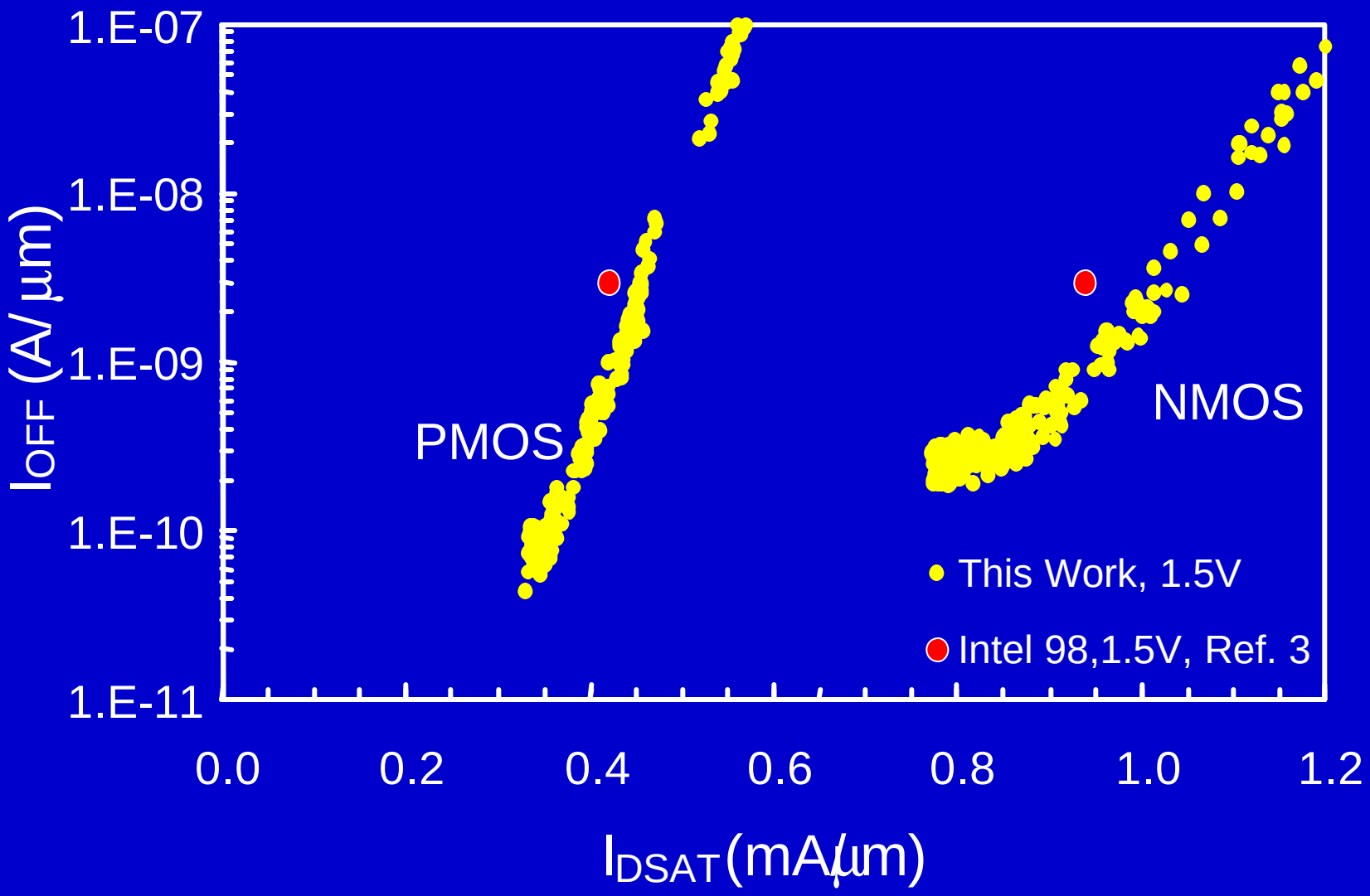
# $I_{ON}$ vs $I_{OFF}$

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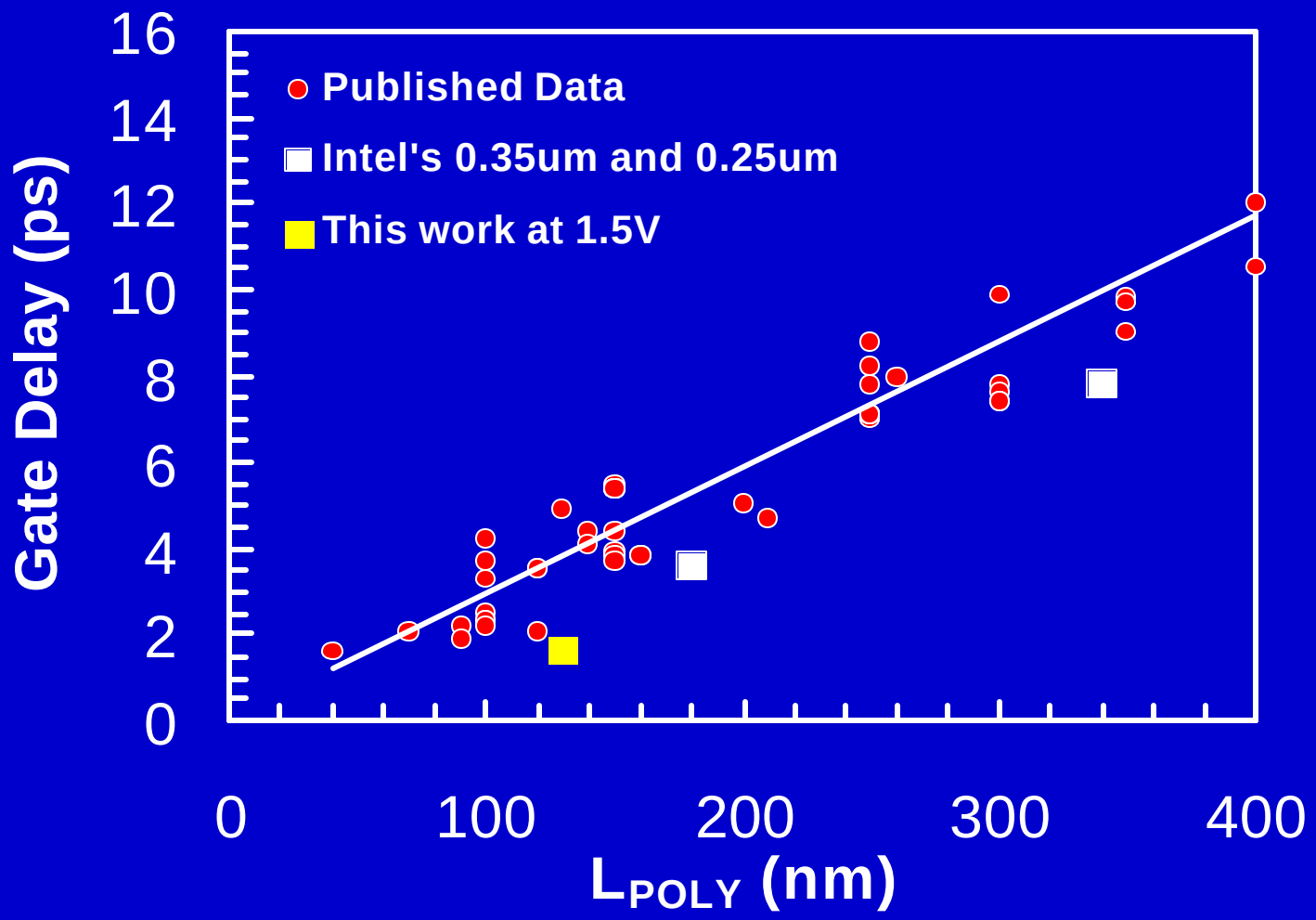
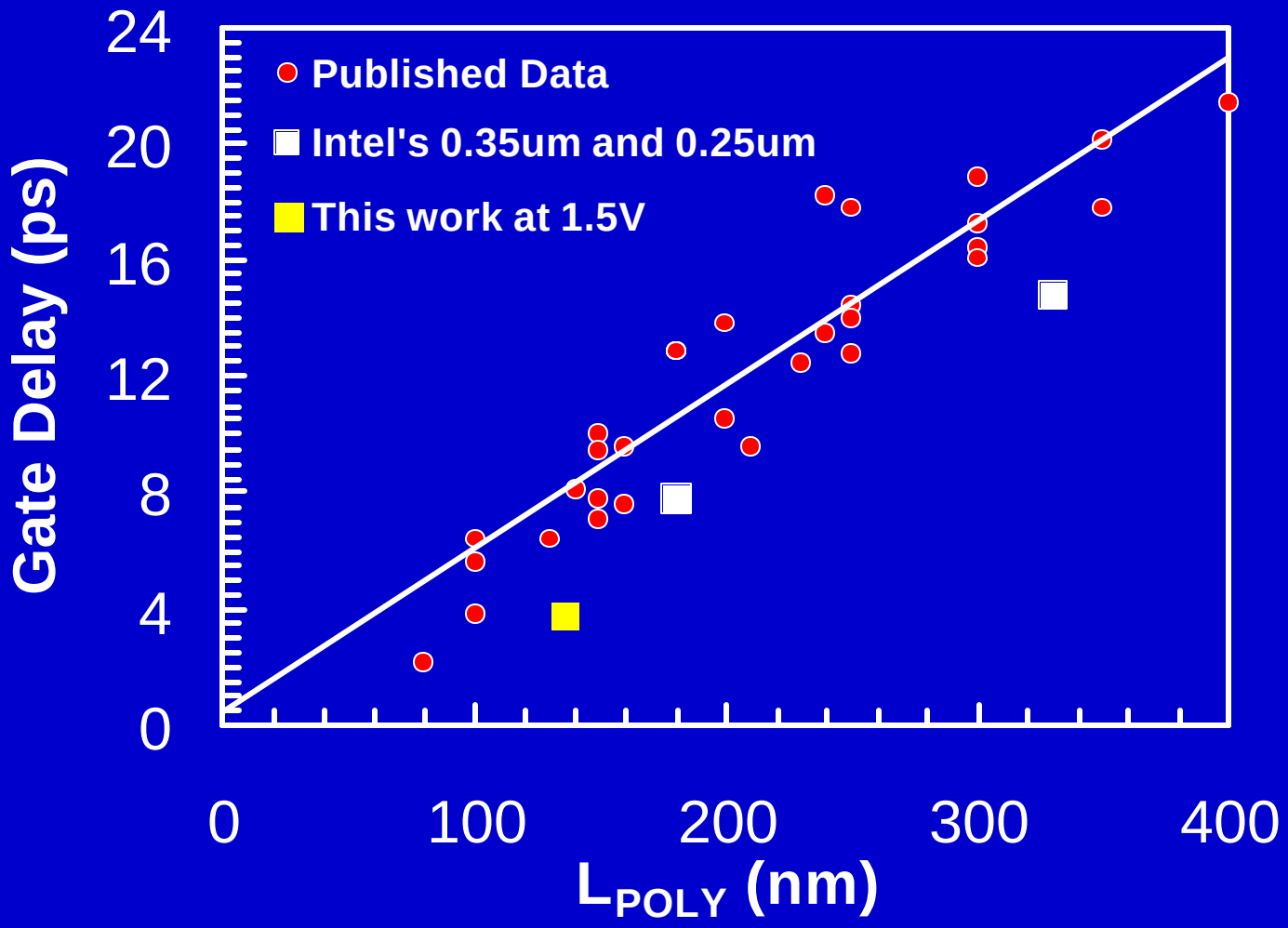
# NMOS CV/I Gate Delay




- NMOS CV/I Delay at 3nA/μm $I_{OFF}$ is 1.65 psec

# PMOS CV/I Gate Delay




- PMOS CV/I Delay at 3nA/µm $I_{OFF}$ is 3.78 psec

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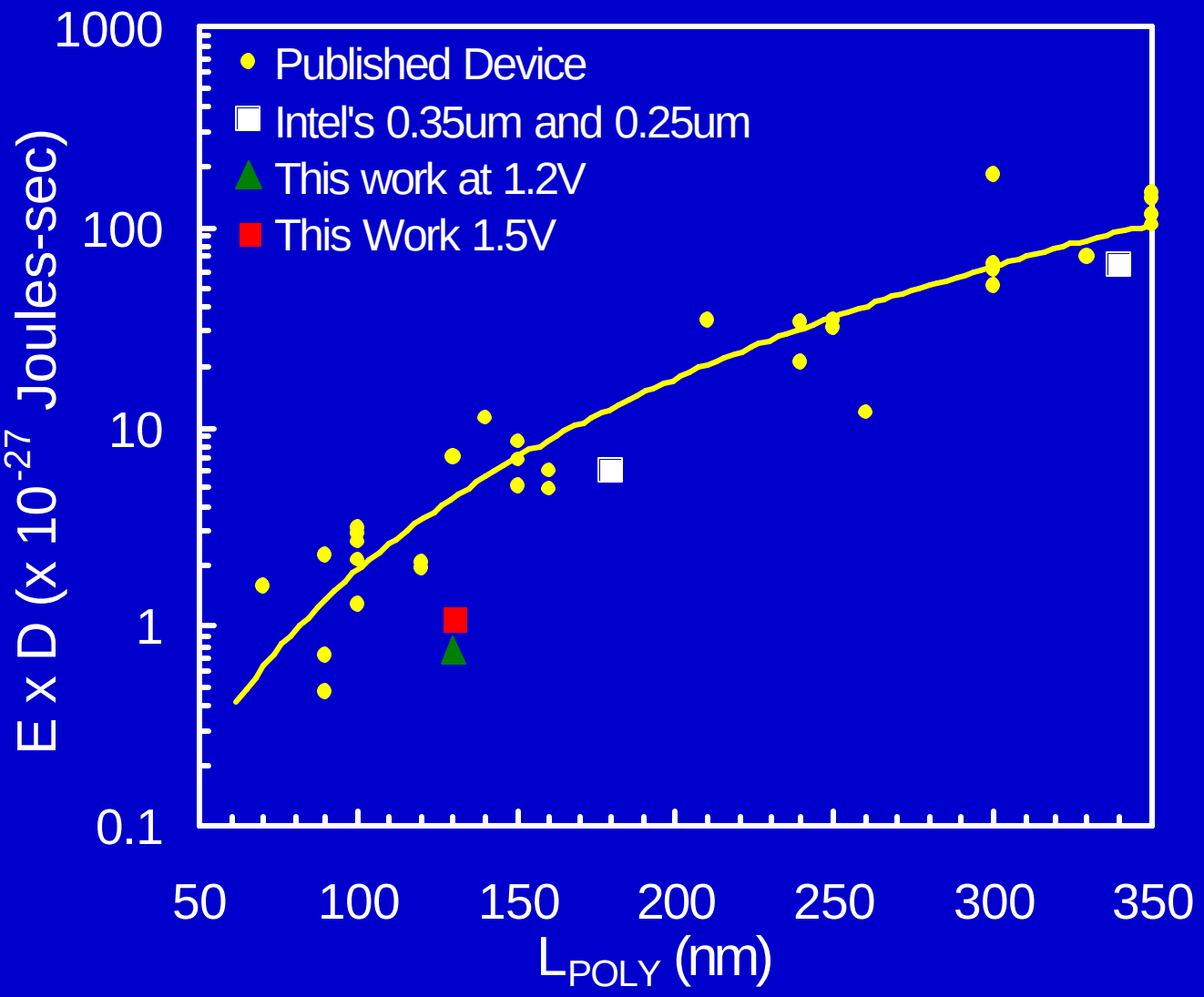
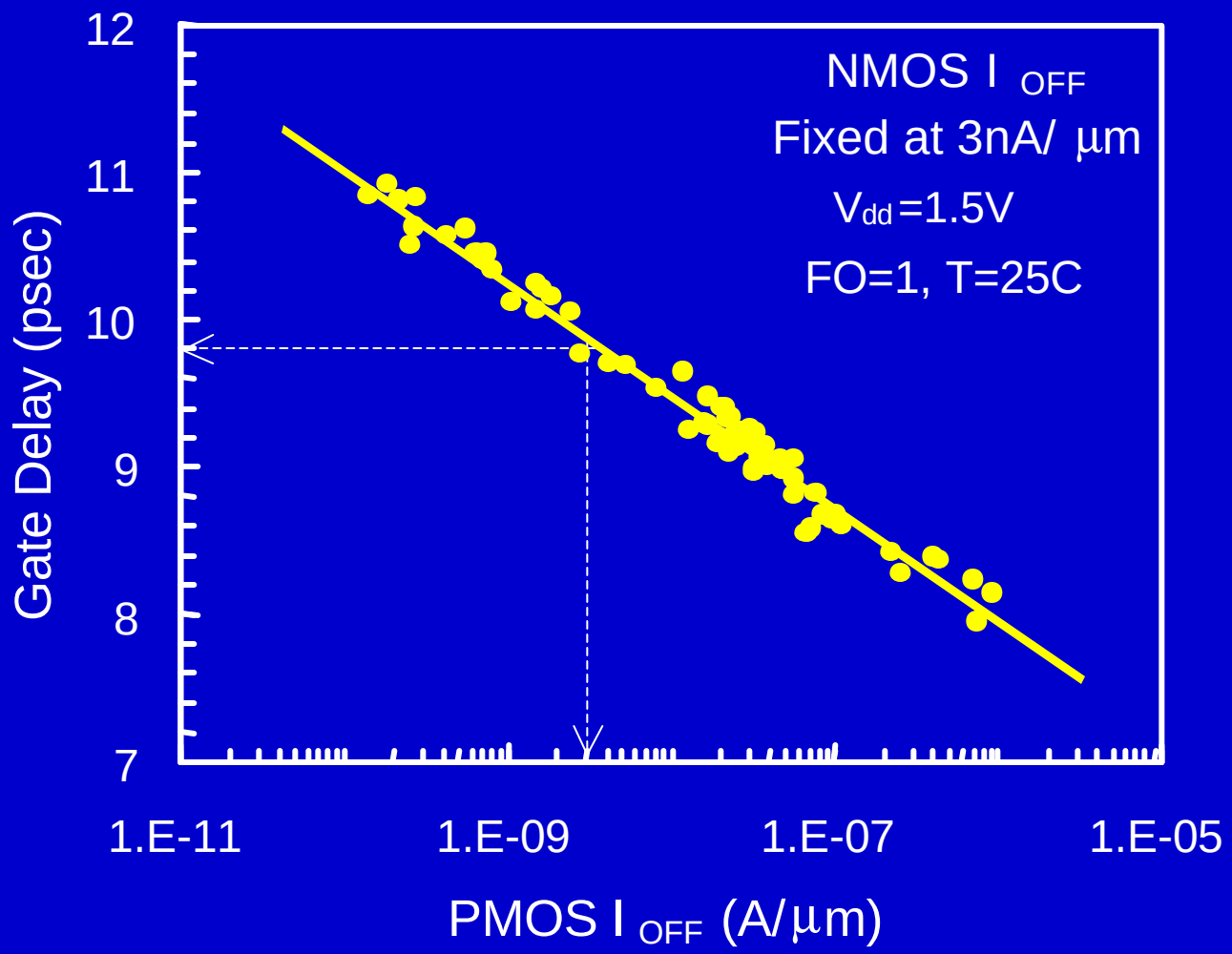
# NMOS Energy x Delay



# Ring Oscillator Delay per Stage

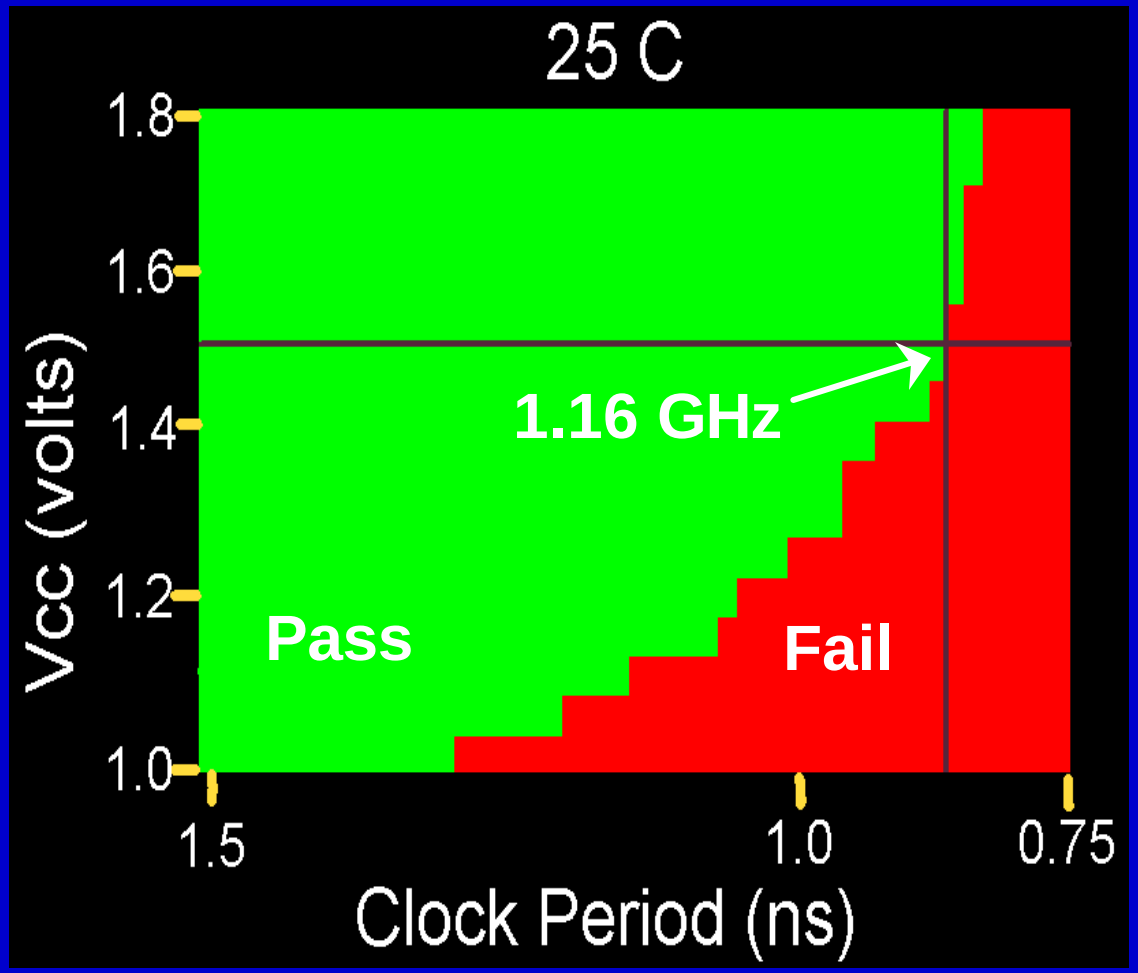



- Sub-10 psec RO delay measured at 1.5V at 3nA/m $I_{OFF}$

# 16 Mbit SRAM Shmoo Plots

- >100 million transistors
- 1.16 GHz SRAM @ 1.5V
- > 800MHz Pentium® III Microprocessors

***(More details at ISSCC '2000)***



# Conclusions

- High performance/low power 100nm $L_{GATE}$ transistor structure presented.
- The best reported $I_{on}$ vs $I_{off}$ characteristics at 1.5V.
- Performance trend better than industry in CV/I and ExD metrics.
- Sub 10ps inverter delay at very moderate $I_{OFF}$ demonstrated.
- 16 MB SRAM yield learning vehicle operates at 1.16 GHz.
- These transistors incorporated in Intel's 180nm logic technology

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